

Customer No.: 31561
Application No.: 10/708,171
Docket NO.: 12681-US-PA

AMENDMENTS

In The Claims:

1. (currently amended) An electro-static discharge (ESD) protection circuit for a dual polarity input/output (I/O) pad, comprising:

a substrate of a first conductive type;

a deep well region of a second conductive type, disposed in the substrate of the first conductive type;

a well region of the first conductive type, disposed in the deep well region of the second conductive type;

a first transistor, disposed over the well region of the first conductive type, wherein the first transistor comprises a first gate, a first source and a first drain;

a second transistor, disposed over the substrate of the first conductive type, wherein the second transistor comprises a second gate, a second source and a second drain, wherein the second source and the first drain are a common-use doped region, and the common-use doped region is overlapping with the deep well region, the well region, and a portion of the substrate other than the deep well region; is connected with the first drain, and wherein the second source and the first drain is disposed in a portion of the first conductive type well region, a portion of the second conductive type deep well region and a portion of the first conductive type substrate;

a first doped region with the first conductive type, disposed in the well region of first conductive type and laterally adjacent to the first source, wherein the first doped region, the first source and the first gate are electrically connected to an input pad; and

Customer No.: 31561
Application No.: 10/708,171
Docket NO.: 12681-US-PA

a second doped region with the first conductive type, disposed in the substrate of the first conductive type and laterally adjacent to the second drain, wherein the second doped region, the second drain and the second gate are electrically connected to an output pad.

2. (previously presented) The electro-static discharge (ESD) protection circuit of claim 1, wherein the substrate of first conductive type comprises a p-type substrate.

3. (previously presented) The electro-static discharge (ESD) protection circuit of claim 1, wherein the deep well region of second conductive type comprises a n-type deep well region.

4. (previously presented) The electro-static discharge (ESD) protection circuit of claim 1, wherein the well region of first conductive type comprises a p-type well region.

5. (original) The electro-static discharge (ESD) protection circuit of claim 1, wherein the first transistor and the second transistor comprise a NMOS transistor.

6. (original) The electro-static discharge (ESD) protection circuit of claim 1, wherein the first doped region and the second doped region comprise a p-type doped region.

7. (previously presented) The electro-static discharge (ESD) protection circuit of claim 1, wherein when the input pad receives a positive electro-static current, a first parasitic bipolar junction transistor is formed by the first conductive type well region, the second type deep well region and the first conductive type substrate, and a second parasitic bipolar junction transistor is formed by the second conductive type deep well region, the first conductive type substrate and the second drain, and a positive feedback loop is formed by the first parasitic bipolar junction transistor and the second parasitic bipolar junction transistor.

8. (previously presented) The electro-static discharge (ESD) protection circuit of claim 1,

Customer No.: 31561
Application No.: 10/708,171
Docket NO.: 12681-US-PA

wherein when the input pad receives a negative electro-static current, a first parasitic bipolar junction transistor is formed by the first conductive type substrate, the second conductive type deep well region and the first conductive type well region, and a second parasitic bipolar junction transistor is formed by the second conductive type deep well region, the first conductive type well region and the first source, and a positive feedback loop is formed by the first parasitic bipolar junction transistor and the second parasitic bipolar junction transistor.